# EXHIBIT 6

IN THE UNITED STATES DISTRICT COURT
FOR THE WESTERN DISTRICT OF TEXAS

VLSI TECHNOLOGY LLC,

Plaintiff,

v.

INTEL CORPORATION,

Defendant.

Civil Action No.: 19-cv-00977-ADA

**DECLARATION OF DR. ALYSSA B. APSEL IN SUPPORT OF INTEL CORPORATION'S OPENING CLAIM CONSTRUCTION BRIEF**

# I. INTRODUCTION AND QUALIFICATIONS

1. I have been retained by counsel for Intel as an expert consultant in this litigation, and I offer this declaration to provide the Court with an overview of the technology described in U.S. Patent No. 6,366,522 ("'522 patent") and U.S. Patent No. 7,292,485 ("'485 patent"), and to provide my opinions regarding how a person of ordinary skill in the art would understand the following claim terms:

2. **<u>'522 Patent</u>**

- "regulate [regulating] at least one supply from a power source and an inductance" (all claims)

**<u>'485 Patent</u>**

- "a capacitance structure"
- "precharging means for precharging the capacitance structure to a predetermined voltage prior to a write operation for the second line of memory cells" (claim 17)
- "first coupling means for coupling the power supply terminal to the first power supply line during the write operation for the second line of memory cells" (claim 17)
- "second coupling means for coupling the second supply line to the first capacitance structure during the write operation for the second line of memory cells" (claim 17)
- "decoupling means for decoupling the first power supply line from the second line of memory cells during the write operation for the second line of memory cells" (claim 17)

3. I received a Ph.D. in Electrical and Computer Engineering from Johns Hopkins University in 2002 and an M.S. from the California Institute of Technology in 1996. I received my B.S. in Electrical Engineering from Swarthmore College in 1995.

4. I am currently the Director of Electrical and Computer Engineering at Cornell University. I was also a co-founder of Alphawave, a start-up designing IP cores for high performance IO and low power RF. The focus of my research is power aware mixed signal

electronics. I have taught undergraduate electronics and circuit design for more than 15 years. I have broad expertise in integrated circuit design including design of integrated power regulators. I have published three papers directly on innovations in power regulator design in top conferences and journals and have worked on design of several others power regulators as components of RF and mixed signal systems. I am also currently working on advanced memory technologies as an alternative technology to SRAM and have two accepted papers on innovations related to the use of spintronics as a non-volatile on-chip solution. This research involves designing baseline SRAM arrays for benchmarking. I am also active in my professional society and currently a Distinguished Lecturer of the IEEE Circuits and Systems society and am Deputy Editor of Circuits and Systems magazine.

5. My C.V. is attached hereto as Exhibit A.

## II. LEGAL STANDARDS

6. I am not an attorney. For the purposes of this declaration, I have been informed about certain aspects of the law that are relevant to my opinions. My understanding of the law is as follow.

7. I have been informed and understand that the terms of a patent are generally given their ordinary and customary meaning, which is the meaning that the term would have to a person of ordinary skill in the art at the time of the claimed invention, which is the time at which the application for the patent was filed.

8. I have been informed and understand that a claim term should be construed in the context of the claim as a whole. I also understand that the specification of the patent is relevant to a claim term's meaning and that a claim term must be read in light of the specification.

9. I have been informed and understand that a patent specification may provide a special definition for a claim term by the patentee that is not the same as the meaning it would

otherwise have. When that is the case, the inventor's lexicography controls the claim term's meaning. In other cases, the specification may contain an intentional disclaimer or disavowal of claim scope by the inventor. When that is the case, the inventor's dictation of the claim scope, as reflected in the specification, controls the meaning of the claim term. I understand that when a patentee describes the features of the "present invention," that description may limit the scope of the invention.

10. I have been informed and understand that a patent's file history, including any reexamination history, may also be relevant to the meaning of a patent's claims, as the file history can reveal evidence of how the U.S. Patent and Trademark Office and the applicant understood the patent and the meaning of patent's terms.

11. I have been informed and understand that the claim language, specification, and prosecution history are referred to as "intrinsic evidence."

12. I have been informed and understand that when a patentee unequivocally and unambiguously disavows a certain meaning to obtain a patent during prosecution or reexamination, the doctrine of prosecution history disclaimer narrows the meaning of the claim consistent with the scope of the claim surrendered.

13. I have been informed and understand that a patent claim is indefinite if the claim, specification, and file history, would fail to inform, with reasonable certainty, the scope of the claimed invention to those skilled in the art.

14. I have been informed and understand that the terms in the claims of patents are required by statute to be definite. While terms do not need to be defined with mathematical precision, I have been informed and understand that the terms of a claim must inform one of ordinary skill in the art about the scope of the terms and the scope of the invention with reasonable

certainty. I have been informed and understand that a term is indefinite if it does not provide one of ordinary skill in the art with reasonable certainty about the scope of the term. I further understand that the specification and prosecution history can be used to determine whether a claim term is definite because the specification and prosecution history can inform the meaning and scope of a term.

15. I have been informed and understand that, where a claim limitation expresses a means or step for performing a specified function without the recital of structure, material, or acts in support thereof, the limitation shall be construed to cover the corresponding structure, material, or acts described in the specification or equivalents thereof, and this is known as a "means-plus-function" limitation. I have been informed and understand that if the specification contains no corresponding structure that is clearly linked to and capable of performing the function recited by the means-plus-function limitation, then the claim is indefinite.

16. I have been informed and understand that patents contain both "independent" and "dependent" claims. I have been informed and understand that a dependent claim includes the features of one or more other claims and should be construed as including all the limitations contained in the claim to which it refers.

## III. '522 PATENT

### A. Technology Background

17. A "voltage regulator" is a component that is designed to maintain a constant controlled voltage in the presence of a changing output "load." It receives an input voltage[1] at one level and uses regulating circuitry to generate an output voltage at a different level. For example,

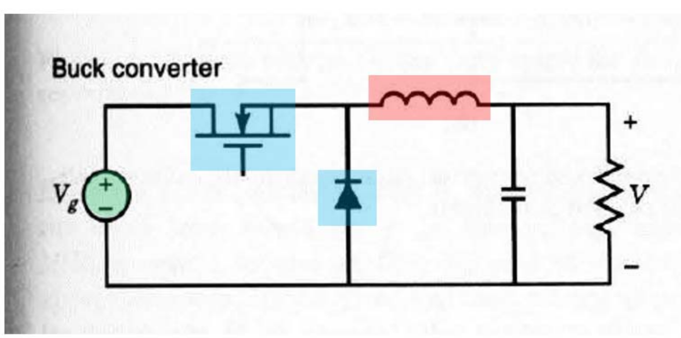
[1] "Voltage" is the measure of electric potential between two points in a circuit, which is analogous to water pressure in a pipe.

a voltage regulator can receive a 5 volt input voltage from the power source (such as a battery), and output a different regulated voltage, such as 2 volts.

18. A common type of voltage regulator, known long before the '522 patent, is a switching regulator. A switching regulator uses a switching device (often implemented using transistors), that alternately connects and disconnects the output to an input power source at a given rate to ultimately provide a regulated voltage at a desired voltage level. A switching regulator that outputs a voltage ***higher*** than the input voltage is called a "boost regulator" or "boost converter," while a voltage regulator that outputs a voltage ***lower*** than the input voltage is called a "buck regulator" or a "buck converter." *See, e.g.*, DX-18 [Erickson] at 53-56. A buck converter is sometimes also referred to as a "down converter."

19. Both boost and buck regulators utilize an "inductor," which is a basic circuit component used in switching regulators (among many other circuits). In general, when electrical current flows through an inductor, the inductor stores energy in the form of a magnetic field, which is referred to as its "inductance."

20. While both boost and buck regulators use inductance, they do so in different ways and for different purposes. A buck regulator uses an inductance at the ***output*** of the regulator (as indicated by the symbol highlighted in red):

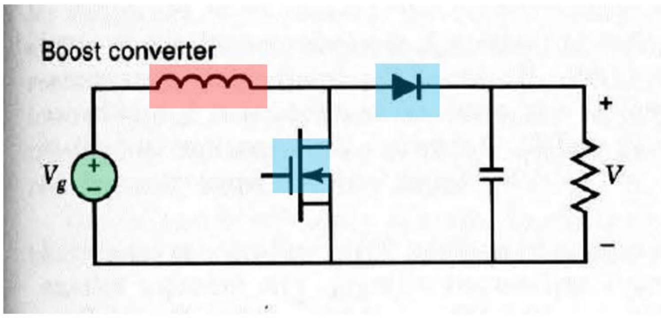



Input voltage: 2 V Output voltage: 1 V

DX-18 [Erickson] at 55, Fig. 4 (annotations added).

21. In the buck regulator shown above, the power source is highlighted in green. For example, the power source can be a battery that provides two volts. The regulating circuitry is highlighted in blue. In the buck regulator shown above, the regulating circuitry consists of a single switch and a diode that acts like a switch (although two or more switches may be used in other implementations). The transistor switch will repeatedly open and close at a determined rate. This causes the left side of the inductor to alternate between the input voltage (when the switch is closed and conducting) and a low voltage (when the switch is open). The changing voltage results in a current through the inductor that alternatively increases and decreases each cycle to match the load at a desired output voltage. The inductor, often in combination with a capacitor, "smooths" out this output voltage to a steady voltage. In other words, in the case of a buck regulator, the inductor stores energy and delivers this to the load to "smooth out" the chopped voltage waveform to a steady voltage level (such as 1 volt).

22. On the other hand, a boost regulator uses an inductance as part of the ***input*** to the regulating circuitry, as shown below.




Input voltage: 2 V

Output voltage: 3 V

DX-18 [Erickson] at 55, Fig. 4 (annotations added).

23. In the boost regulator shown above, the inductor (in red) is connected to the power source (in green), and is thus located between the power source and the regulating switch and diode (in blue). In other words, in case of a boost regulator, the inductor is positioned on the ***opposite*** side of the regulating circuity as compared to a buck regulator.

24. The purpose of the inductor in a boost regulator is also different from a buck regulator. In a boost regulator, the inductor functions to add energy to the system so that the output voltage will be higher than the input voltage. When the regulating switch is closed, a current will flow through the inductor to ground, thereby building up energy in a magnetic field in the inductor. When the regulating switch opens, some of that extra built-up energy in the inductor will be combined with the energy from the input voltage and transferred to the output of the circuit. By repeating this cycle, the output voltage will end up being at a "boosted," or higher, output voltage (for example, three volts). Thus, unlike a buck regulator, the inductance in a boost regulator is connected to the power source and positioned between the power source and regulating circuitry.

**B. Level of Ordinary Skill In The Art**

25. Based on my review of the '522 patent, the '522 patent describes a power management approach for integrated circuits by controlling voltage and clock frequency based on processor need. DX-1 ['522 patent] at 1:45-48. Based on my review of the patent and my familiarity with the technology described in the patent, a person of ordinary skill in the art at the time of the alleged invention of the '522 patent would have had at least (1) an undergraduate degree in electrical engineering (or an equivalent subject), together with three years of post-graduate experience designing power management circuits; or (2) a master's degree in electrical engineering (or equivalent subject) together with two years of post-graduate experience designing power management circuits. This description is approximate, and a higher level of education or skill

might make up for less experience, and vice-versa. I was as at least a person of ordinary skill in the art as of November 20, 2000.

## C. OVERVIEW OF THE '522 PATENT

### 1. Background

26. The '522 patent issued on April 2, 2002, from an application filed on November 20, 2000. The '522 patent is generally directed to controlling power consumption in an integrated circuit. *See, e.g.*, DX-1 ['522 patent], Abstract ("A method and apparatus for controlling power consumption of an integrated circuit . . . ").

### 2. Stated Problem

27. According to the '522 patent, the purported problem in the prior art was that microprocessors could only provide a fixed supply voltage and system clock frequency, which resulted in wasted power when not executing demanding software applications. Specifically, the patent explains that microprocessors handle a variety of software applications, some of which that "push the processing engine to its processing speed limits" while "most applications do not." *Id.* at 1:33-35. "However, the processing engine must be designed to support the highest processing requirements" and "needs to have a supply voltage and system clock to handle the most taxing applications." *Id.* at 1:35-37. According to the patent, microprocessors would have to maintain the voltage and system clock settings to support the most demanding applications, even when executing less taxing applications. *Id.* at 1:39-44. The patent states that "[a] need exists for a method and apparatus that adjust the system clock and/or the supply voltage based on the processing capabilities of the integrated circuit and the application being performed to conserve power." *Id.* at 1:45-48.

### 3. Summary of the Alleged Invention

28. The '522 patent's alleged solution is to dynamically adjust the voltage and clock frequency "based on the processing capabilities of the integrated circuit and the application being performed to conserve power." *Id.* at 1:45-48. Claim 1 recites:

> 1. A power efficient integrated circuit comprising:
>
> > [a] phase lock loop operably coupled to receive a reference clock and to produce therefrom a system clock based on a system clock control signal;
> >
> > [b] on-chip power supply control module operably coupled to regulate at least one supply from a power source and an inductance based on a power supply control signal;
> >
> > [c] memory operably coupled to store at least one application; and
> >
> > [d] computational engine operably coupled to produce the system clock control signal and the power supply control signal based on a processing transfer characteristic of the computation engine and processing requirements associated with processing at least a portion of the at least one application.

29. As shown above, limitation [b] of claim 1 recites an "on-chip power supply control operably coupled to regulate at least one supply from a power source and an inductance based on a power supply control signal," which includes the disputed term discussed below.

## D. Disputed term: "regulate [regulating] at least one supply from a power source and an inductance" (all claims)

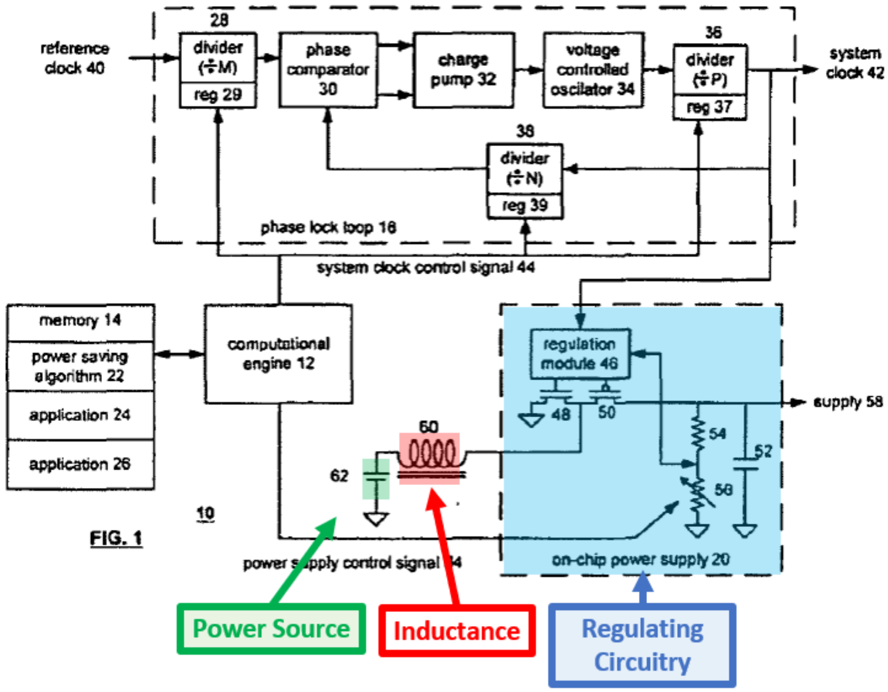
30. I understand that Intel has proposed that this term be construed to mean "regulate [regulating] at least one supply from an inductance connected to a power source, where the

inductance is positioned between the power source and the regulating circuitry," and that VLSI has proposed that this term be construed to have its "plain and ordinary meaning."

31. As I explain below, Intel's proposed construction is supported by the patentee's statements made to the Patent Office during reexamination. VLSI's proposed construction, which does not provide any definition beyond "plain and ordinary meaning," does not take into account the patentee's statements during reexamination.

32. During reexamination, the examiner rejected claim 1, which included the term in dispute, in view of eight prior references, each of which disclosed a "buck converter" or "down converter." In particular, the examiner found that the buck converters disclosed in Dancy, Min, Wei, Goodman, Burd I, Burd II, Gutnik I, and Gutnik II satisfied the "inductance limitation" of claim 1 because they are all "directed to the concept of using an inductance-based regulator." DX-10 [5/6/2008 Rejection] at 55-58.

33. In response to these rejections, the patentee explained that "claim 1 recites 'A power efficient integrated circuit comprising . . . on-chip power supply control module operably coupled to regulate at least one supply *from a power source and an inductance* based on a power supply control signal (emphasis added).'" DX-11 [7/16/2008 Reply] at 16 (emphasis in original). The patentee then explained, in reference to Figure 1 of the '522 patent, that "[t]his limitation is supported in the '522 patent by, inter alia, on-chip power supply 20, which regulates supply 58 from power source 62 (e.g. a battery) *and* inductance 60[.]" *Id.* at 16 (emphasis in original). Figure 1 of the '522, reproduced in annotated form below, shows a typical boost regulator configuration:




*Id.*, '522 Fig. 1 (annotations added). As shown above, Figure 1 shows a boost regulator where the inductance (in red) is connected to the power source (in green), and is positioned between the power source and the regulating circuitry (in blue).

34. To contrast Figure 1 of the '522 patent from Dancy, the patentee reproduced Figure 10 from Dancy and explained that "Dancy's regulator ('Down Converter'), however, does not regulate at least one supply (Vout) 'from a power source and an inductance' because the power supply control signal operates switches S1 and S2 from the power source (Vin) alone, not from the power source and the inductance as recited in claim 1[.]" DX-11 [7/17/2008 Reply] at 16.

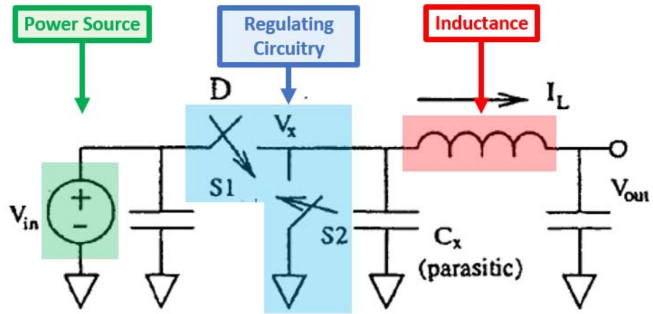



**Figure 10:** Standard Down Converter Topology.

*Id.*, Dancy Figure 10 (annotations added).

35. As shown above, Dancy Figure 10 shows a "Standard Down Converter," which is synonymous with a buck converter. A person of ordinary skill at the time of the application would understand that Dancy Figure 10 has the characteristics of a typical buck converter, where the inductance (in red) is positioned after the regulating circuitry (in blue). As explained by the patentee, "switches S1 and S2" in Dancy's buck converter regulate "from the power source (Vin) alone," instead of regulating from ***both*** a power source and an inductance, which would be the case in a boost converter, where the inductance is connected to the power source and positioned between the power source and the regulating circuitry (as shown, for example, in Figure 1 of the '522 patent).

36. Next, the patentee distinguished Min on the same basis. Specifically, the patentee reproduced Figure 3 of Min and explained that "claim 1 recites 'A power efficient integrated circuit comprising . . . on-chip power supply control module operably coupled to regulate at least one supply *from a power source and an inductance* based on a power supply control signal (emphasis added).' Min's inductance is not connected to a power source and Min does not disclose regulating Vout 'from a power source and an inductance'[.]" *Id.* at 22-23 (emphasis in original).

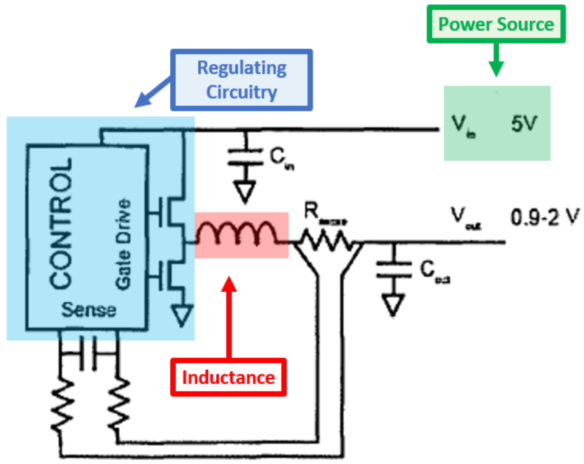
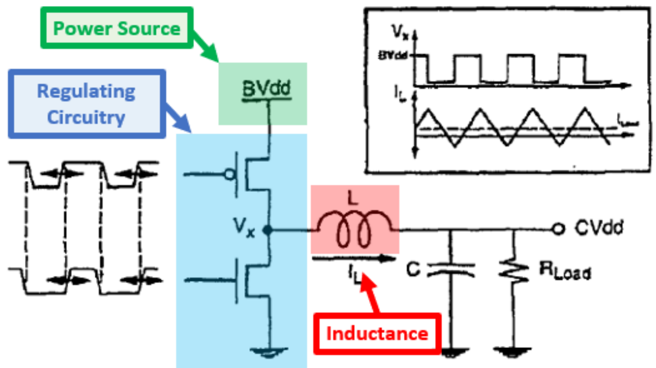



**Figure 3.** Simplified schematic for the buck regulator.

*Id.* at 23, Min Figure 3 (annotations added).

37. As shown above, Min Figure 3 shows a "[s]implified schematic for the buck regulator." *Id.* at 23, Min Figure 3. A person of ordinary skill at the time of the application would understand that Min Figure 3 has the characteristics of a typical buck converter, where the inductance (in red) is positioned after the regulating circuitry (in blue). As explained by the patentee, "Min's inductance is not connected to a power source." *Id.* at 22-23. In contrast, in a boost converter, the inductance ***is*** connected to the power source and thus positioned between the power source and the regulating circuitry (as shown, for example, in Figure 1 of the '522 patent).

38. Next, the patentee distinguished Wei on the same basis. Specifically, the patentee reproduced Figure 1 of Wei and explained that "claim 1 recites 'A power efficient integrated circuit comprising . . . on-chip power supply control module operably coupled to regulate at least one supply *from a power source and an inductance* based on a power supply control signal (emphasis added).' Wei's inductance is not connected to a power source and Wei does not disclose regulating CVdd 'from a power source and an inductance'[.]" *Id.* at 25-26 (emphasis in original).




*Id.* at 26, Wei Figure 1 (annotations added).

39. As shown above, Wei Figure 1 shows a "Buck Converter." A person of ordinary skill in the art at the time of the application would understand that Wei Figure 1 has the characteristics of a typical buck converter, where the inductance (in red) is positioned after the regulating circuitry (in blue). As explained by the patentee, "Wei's inductance is not connected to a power source." *Id.* at 25-26. In contrast, in a boost converter, the inductance ***is*** connected to the power source and thus positioned between the power source and the regulating circuitry (as shown, for example, in Figure 1 of the '522 patent).

40. Next, the patentee distinguished Goodman on the same basis. Specifically, the patentee reproduced Figure 2 of Goodman and explained that "claim 1 recites 'A power efficient integrated circuit comprising . . . on-chip power supply control module operably coupled to regulate at least one supply *from a power source and an inductance* based on a power supply control signal (emphasis added).' Goodman's 'external LC filter' is not connected to a power source and Goodman does not disclose regulating $V_{DD}/V_{A/D}$ 'from a power source and an inductance' . . . Goodman's DC/DC converter in fact uses the external LC filter in a synchronous buck configuration." *Id.* at 29 (emphasis in original).

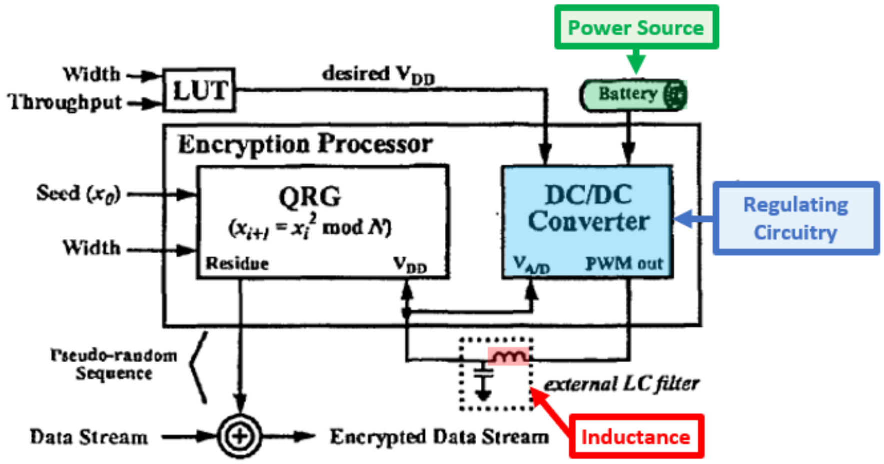



Fig. 2. System architecture of the scalable encryption processor.

*Id.* at 26, Goodman Figure 2 (annotations added).

41. As explained by the patentee, Goodman Figure 2 shows a "synchronous buck configuration." *Id.* at 29. A person of ordinary skill at the time of the application would understand that Goodman Figure 2 has the characteristics of a typical buck converter, where the inductance (in red) is positioned after the regulating circuitry (in blue). As explained by the patentee, "Goodman's 'external LC filter' is not connected to a power source." *Id.* at 29. A buck converter often uses an LC filter (which comprises an inductor L and a capacitor C) at the output of the regulating circuitry to smooth out the output voltage. In contrast, in a boost converter, the inductance is connected to the power source at the input to the regulating circuitry, and thus positioned between the power source and the regulating circuitry (as shown, for example, in Figure 1 of the '522 patent).

42. Next, the patentee distinguished Burd I on the same basis. Specifically, the patentee reproduced Figure 17.4.2 of Burd I and explained that "claim 1 recites 'A power efficient integrated circuit comprising . . . on-chip power supply control module operably coupled to regulate at least one supply *from a power source and an inductance* based on a power supply

control signal (emphasis added).' Burd I's DC/DC converter is implemented with a regulator and an external inductor and capacitor, and Burd I not disclose regulating $V_{DD}$ 'from a power source and an inductance' . . . Burd I's DC/DC converter in fact uses the external LC filter in a synchronous buck configuration." *Id.* at 32 (emphasis in original).

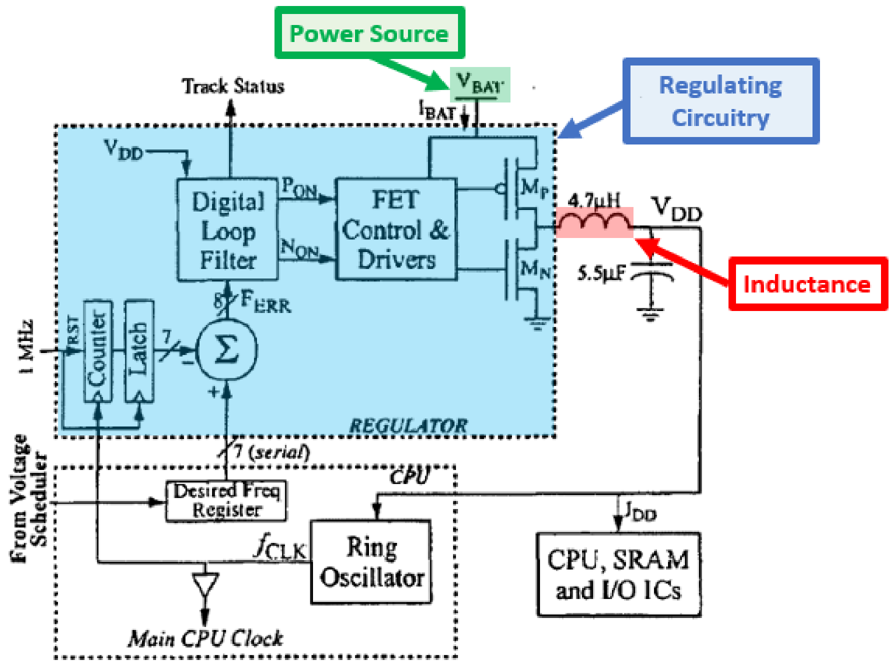



**Figure 17.4.2: Frequency to voltage feedback loop.**

*Id.* at 32, Burd I Figure 17.4.2 (annotations added).

43. As explained by the patentee, Burd I Figure 17.4.2 shows a "synchronous buck configuration." *Id.* at 32. A person of ordinary skill at the time of the application would understand that Burd I Figure 17.4.2 has the characteristics of a typical buck converter, where the inductance (in red) is positioned after the regulating circuitry (in blue). As explained by the patentee, Burd I uses an "external LC filter in a synchronous buck configuration." *Id.* at 32. A buck converter often uses an LC filter (which comprises an inductor L and capacitor C) at the output of the regulating circuitry to smooth out the output voltage. In contrast, in a boost converter, the inductance is connected to the power source at the input to the regulating circuitry, and thus

positioned between the power source and the regulating circuitry (as shown, for example, in Figure 1 of the '522 patent).

44. Next, the patentee distinguished Burd II on the same basis. Specifically, the patentee reproduced Figure 7 of Burd II and explained that "claim 1 recites 'A power efficient integrated circuit comprising . . . on-chip power supply control module operably coupled to regulate at least one supply *from a power source and an inductance* based on a power supply control signal (emphasis added).' The DC/DC converter of Burd II is implemented with a regulator and an external inductor and capacitor, and Burd II not disclose regulating $V_{DD}$ 'from a power source and an inductance' . . . Burd II's DC/DC converter in fact uses the external LC filter in a synchronous buck configuration." *Id.* at 35-36 (emphasis in original).

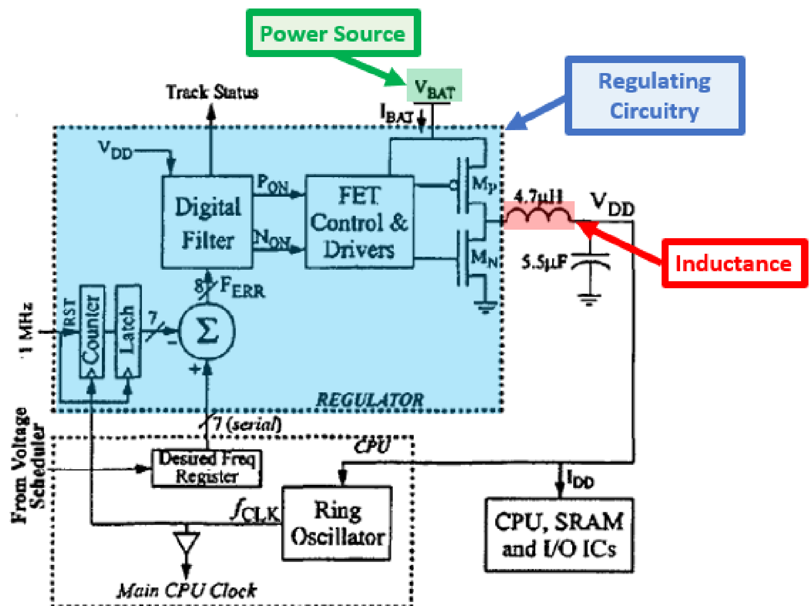



Fig. 7. Frequency to voltage feedback loop.

*Id.* at 36, Burd II Figure 7 (annotations added).

45. As explained by the patentee, Burd II Figure 7 shows a "synchronous buck configuration." *Id.* at 36. A person of ordinary skill at the time of the application would understand that Burd II Figure 7 has the characteristics of a typical buck converter, where the inductance (in

red) is positioned after the regulating circuitry (in blue). As explained by the patentee, Burd I uses an "external LC filter in a synchronous buck configuration." *Id.* at 36. A buck converter often uses an LC filter (which comprises an inductor L and capacitor C) at the output of the regulating circuitry to smooth out the output voltage. In contrast, in a boost converter, the inductance is connected to the power source at the input of the regulating circuitry, and thus positioned between the power source and the regulating circuitry (as shown, for example, in Figure 1 of the '522 patent).

46. Next, the patentee distinguished Gutnik I on the same basis. Specifically, the patentee reproduced Figure 8 of Gutnik I and explained that "claim 1 recites 'A power efficient integrated circuit comprising . . . on-chip power supply control module operably coupled to regulate at least one supply *from a power source and an inductance* based on a power supply control signal (emphasis added).' Gutnik I discloses a buck converter using an inductor and capacitor, and Gutnik I does not disclose regulating $V_{out}$ 'from a power source and an inductance'[.]" *Id.* at 39 (emphasis in original).

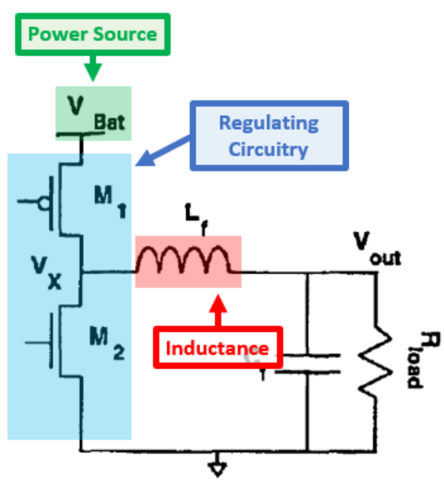



Fig. 8. Simplified buck converter schematic.

*Id.* at 39, Gutnik I Figure 8 (annotations added).

47. As explained by the patentee, Gutnik I Figure 8 shows "a buck converter using an inductor and capacitor." *Id.* at 39. A person of ordinary skill at the time of the application would understand that Gutnik I Figure 8 has the characteristics of a typical buck converter, where the inductance (in red) is positioned after the regulating circuitry (in blue). In contrast, in a boost converter, the inductance is connected to the power source and thus positioned between the power source and the regulating circuitry (as shown, for example, in Figure 1 of the '522 patent).

48. Finally, the patentee distinguished Gutnik II on the same basis. Specifically, the patentee reproduced Figure 6 of Gutnik II and explained that "claim 1 recites 'A power efficient integrated circuit comprising . . . on-chip power supply control module operably coupled to regulate at least one supply *from a power source and an inductance* based on a power supply control signal (emphasis added).' The DC/DC converter of Gutnik II is implemented with a PWM controller, driver, and an inductor and capacitor, and Gutnik II does not disclose regulating $V_{out}$ 'from a power source and an inductance' . . . Gutnik II's DC/DC converter uses the LC filter in a buck configuration, but doesn't regulate a supply voltage 'from an inductance and a power source.'" *Id.* at 42-43 (emphasis in original).

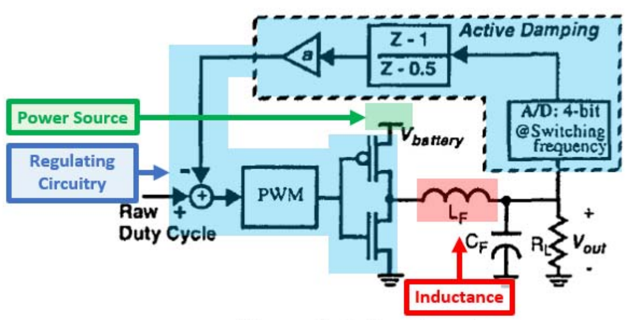


Figure 6: Active Damping

*Id.* at 43, Gutnik II Figure 6 (annotations added).

49. As explained by the patentee, Gutnik II Figure 6 shows a "buck configuration." *Id.* at 43. A person of ordinary skill at the time of the application would understand that Gutnik II

Figure 6 has the characteristics of a typical buck converter, where the inductance (in red) is positioned after the regulating circuitry (in blue). As explained by the patentee, Gutnik II uses "the LC filter in a buck configuration, but doesn't regulate supply voltage 'from an inductance and a power source.'" *Id.* at 43. A buck converter uses an LC filter (which comprises an inductor L and capacitor C) at the output of the regulating circuitry to smooth out the output voltage. In contrast, in a boost converter, the inductance is connected to the power source and the input of the regulating circuitry, and thus positioned between the power source and the regulating circuitry (as shown, for example, in Figure 1 of the '522 patent).

50. In view of the repeated arguments by the patentee to distinguish each of the buck regulator references discussed above, the patentee unmistakably made clear that the term "regulating from a power source and an inductance" requires the inductance to be in a specific position that is a characteristic of boost regulators, and not buck regulators. Specifically, through the repeated statements and figures from the prior art, the patentee unmistakably made clear that the claim term requires that the inductance be connected to the power supply, and that the inductance is therefore positioned between the power source and the regulating circuitry.

51. VLSI's proposed construction is simply "plain and ordinary meaning," which does not capture the requirements that the patentee set forth during reexamination—that the inductance be connected to a power source and be positioned between the power source and regulating circuitry.

52. Accordingly, a person of ordinary skill in the art at the time of the application would understand, from reading the reexamination history, that the term "regulate [regulating] at least one supply from a power source and an inductance" means "regulate [regulating] at least one

supply from an inductance connected to a power source, where the inductance is positioned between the power source and the regulating circuitry."

## IV. '485 PATENT

### A. Technology Background

53. SRAM ("Static Random Access Memory") is a form of computer memory that retains data as long as it is powered. It is "static" because the data does not have to be refreshed at periodic time intervals, and it is "random access memory" because any address within the memory can be written to or read from. In order to store data in an SRAM cell, a voltage supply must be applied to the cell.

54. SRAM is typically structured as an array of memory cells. An array typically includes "lines" of memory cells. Each line consists of multiple memory cells, and each cell can hold one bit of data. A line of memory cells also includes switches, storage elements, conductors and other circuitry that supply voltage to the memory cells and that control the process of writing to and reading from the cells.

55. As the '485 patent acknowledges, there is a trade-off in setting the level of the voltage applied to an SRAM cell. A higher voltage improves the cell's stability, making it less likely to lose stored data. However, a higher voltage also makes it harder to write new data to the cell. Techniques for resolving this tension were well known prior to the '485 patent. One such technique is known as "write assist," in which a "write assist circuit" temporarily lowers the voltage applied to memory cells during write operations and maintains a higher voltage when cells are not being written to.

### B. Level of Ordinary Skill In The Art

56. Based on my review of the '485 patent, the '485 patent describes a write-assist technique for a memory array that lowers the voltage to memory cells being written to by charge

sharing. DX-2 ['485 patent] at 2:6-23. Based on my review of the patent and my familiarity with the technology described in the patent, a person of ordinary skill in the art at the time of the alleged invention of the '485 patent would have had at least (1) an undergraduate degree in electrical engineering (or an equivalent subject), together with three years of post-graduate experience designing memory circuits; or (2) a master's degree in electrical engineering (or equivalent subject) together with two years of post-graduate experience designing memory circuits. This description is approximate, and a higher level of education or skill might make up for less experience, and vice-versa. I was as at least a person of ordinary skill in the art as of July 31, 2006.

### C. OVERVIEW OF THE '485 PATENT

#### 1. Background

57. The '485 patent issued on November 6, 2007, from an application filed on July 31, 2006. The '485 patent is generally directed to a write-assist technique for a memory array that lowers the voltage to memory cells being written to by charge sharing with a "capacitance structure" including "dummy" memory cells. *See, e.g.*, *id.* at 2:6-23.

58. During read operations, the memory cells are coupled to a power supply voltage that provides charge to the memory cells. *Id.* at 4:24-28, 6:7-10. During write operations, a line of memory cells being written to is decoupled from the power supply voltage and coupled instead to a line of dummy cells. *Id.* at 4:33-39, 6:16-22. Virtually all electrical components, including the line of memory cells being written to and the line of dummy cells, can store electrical charge. The ability to store charge is known as capacitance. When the memory cells are coupled to the dummy cells, the charge in the memory cells is distributed across the combined structure, lowering the voltage at the memory cells. *Id.* at 2:14-19, 4:39-44, 6:22-27. The amount by which the voltage is lowered depends on the relative capacitances of the memory cells and the dummy cells.

### 2. Stated Problem

59. The ’485 patent recognized – as was well known in the art – that “improving stability [of a memory cell] comes at the expense of lower write performance.” *Id.* at 1:37-38. The patent states that “there is a need for a SRAM having improved cell stability while also having improved write margins.” *Id.* at 1:42-43.

### 3. Summary of the Alleged Invention

60. The ’485 patent’s alleged solution is a specific technique for lowering the voltage to a line of memory cells by “charge sharing” with a line of “dummy cells.”

61. Claims 1, 12, and 17 recite:

> 1. A memory circuit, comprising:
>
> > [a] a memory array comprising a first line of memory cells and a second line of memory cells;
> >
> > [b] a first power supply terminal;
> >
> > [c] a first capacitance structure includes a plurality of dummy cells;
> >
> > [d] a first power supply line coupled to the first line of memory cells;
> >
> > [e] a second power supply line coupled to the second line of memory cells; and
> >
> > [f] a switching circuit that has transistors that, connected between the first power supply terminal, the first power supply line, the second power supply line and the first capacitance structure wherein when the second line of memory cells is selected for writing, couple the first power supply terminal to the first power supply line, decouple the first power supply terminal from the second line of memory cells, and couple the second power supply line to the first capacitance structure.
>
> 12. A method, comprising:
>
> > [a] providing a memory comprising:
> >
> > > a memory array comprising a first line of memory cells and a second line of memory cells;
> > >
> > > a first power supply terminal;

a first capacitance structure includes a plurality of dummy cells;

a first power supply line coupled to the first line of memory cells; and

a second power supply line coupled to the second line of memory cells;

a switching circuit that has transistors that connected between the first power supply terminal, the first power supply line, the second power supply line and the first capacitance structure

[b] selecting the second line of memory cells for writing;

[c] coupling the first power supply terminal to the first power supply line;

[d] decoupling the second line of memory cells from the first power supply terminal;

[e] coupling charge from the second power supply line to the first capacitance structure; and

[f] writing a memory cell in the second line of memory cells.

17. A memory circuit, comprising:

[a] a memory array comprising a first line of memory cells and a second line of memory cells;

[b]a power supply terminal;

[c] a capacitance structure;

[d] a first power supply line coupled to the first line of memory cells;

[e] a second power supply line coupled to the second line of memory cells;

[f] precharging means for precharging the capacitance structure to a predetermined voltage prior to a write operation for the second line of memory cells;

[g] first coupling means for coupling the power supply terminal to the first power supply line during the write operation for the second line of memory cells;

[h] decoupling means for decoupling the first power supply line from the second line of memory cells during the write operation for the second line of memory cells; and

> [i] second coupling means for coupling the second supply line to the first capacitance structure during the write operation for the second line of memory cells.

**D. Disputed Term: "a capacitance structure" (claims 1, 12, 17)**

62. I understand that Intel has proposed that this term be construed as a means-plus-function claim with a function of "providing capacitance" and a corresponding structure of:

> (1) Dummy column 17 (comprised of dummy SRAM cells 30, 32, and 34 and dummy bitlines SBL and SBL*) and conductor 37, configured to be selectively coupled to one or more of the dummy SRAM cells, as shown in Figure 2, and equivalents thereof; or alternatively (2) dummy row 70 (comprised of dummy SRAM cells 82, 84, and 86 and dummy wordline SWL) and conductor 71, configured to be selectively coupled to one or more dummy of the SRAM cells, as shown in Figure 3, and equivalents thereof

63. I further understand that VLSI has proposed that this term be construed as "plain and ordinary meaning."

64. It has been explained to me that if a claim term fails to recite sufficiently definite structure or recites function without reciting sufficient structure for performing that function, it is construed as a means-plus-function term. I further understand that, in determining the meaning of a means-plus-function term, the court will first look at the function set forth in the claim and then identify the corresponding structure in the patent specification that performs that function.

65. At the time of the '485 patent's filing and continuing through today, the term "capacitance structure" would not connote a definite structure to a person of skill in the art. Instead, a person of skill in the art would recognize the term as simply stating a function – providing capacitance – without reciting any structure for performing that function. Because

virtually every integrated circuit component has some amount of capacitance (parasitic[2] or otherwise), and could therefore be used as the circuit element with which the line of memory cells shares charge as described in the ’485 patent, a person of ordinary skill in the art would not understand the term “capacitance structure” to recite a definite structure.

66. Likewise, neither the specification nor the prosecution history of the ’485 patent attributes any particular meaning to this phrase. Therefore, a person of ordinary skill in the art reading the claims of the ’485 patent at the time of the invention would not understand the term “capacitance structure” to refer to any particular structure, but instead would understand a “capacitance structure” to be any structure used for the function of providing capacitance.

67. The ’485 patent discloses two structures for providing capacitance, a dummy column and a dummy row. *Id.* at 4:3-7, 4:39-55, 6:22-31. The ’485 patent further describes the components that make up the disclosed dummy column and the dummy row. As shown in Figure 2, dummy column 17 is comprised of dummy SRAM cells 30, 32, and 34 and dummy bitlines SBL and SBL*, along with conductor 37 configured to be selectively coupled to one or more of the dummy SRAM cells. *Id.* at 3:59-65 (“Dummy column 17 … includes a pair of dummy bit lines labeled ‘SBL’ and ‘SBL*.’ Dummy SRAM cells 30, 32 and 34 are coupled to the dummy bit lines SBL and SBL* and are conventional SRAM cells …. Each of the dummy cells has a supply terminal that can be coupled to a conductor 37.”).

68. As shown in Figure 3, dummy row 70 is comprised of dummy SRAM cells 82, 84, and 86 and dummy wordline SWL, along with conductor 71 configured to be selectively coupled to one or more dummy of the SRAM cells. *Id.* at 5:39-45 (“Dummy row 70 … includes a word

[2] “Parasitic capacitance” is the capacitance, often unintentional, that exists when charge is stored due to the proximity of electronic components.

line labeled 'SWL' and all of the cells coupled to SWL. Dummy SRAM cells 82, 84, and 86 are coupled to the dummy word line SWL and are conventional SRAM cells …. Each of the dummy cells has a supply terminal that can be coupled to a conductor 71.").

### E. Disputed Term: "precharging means for precharging the capacitance structure to a predetermined voltage prior to a write operation for the second line of memory cells" (claim 17)

69. I understand that the parties agree that this term should be construed as a means-plus-function term and agree that the function is "precharging the capacitance structure to a predetermined voltage prior to a write operation for the second line of memory cells." I understand that the parties disagree, however, as to what structure in the specification of the '485 patent is linked to that function.

70. I understand that Intel has proposed that the corresponding structure is:

> (1) voltage source $V_{REF}$ and transistor 36, coupled in series to provide a reference voltage to one or more dummy cells through conductor 37, as shown in Figure 2, and equivalents thereof; or alternatively (2) voltage source $V_{REF}$ and transistor 90, coupled in series to provide a reference voltage to one or more dummy cells through conductor 71, as shown in Figure 3, and equivalents thereof.

71. The specification clearly links each of the components identified by Intel to the function of precharging, and each component is necessary for precharging. Precharging is the process of setting the amount of charge in the capacitance structure to a predetermined voltage level. The specification describes using a voltage source to provide a reference voltage (i.e., a predetermined voltage). The specification further describes two structures for coupling the dummy cells within the capacitance structure to this reference voltage, both accomplishing the coupling through a transistor and conductor. As the '485 patent explains, precharging occurs only when a control signal "cause[s] transistor 36 to be conductive" so that the reference voltage is supplied to the dummy cells. *Id.* at 4:7-8, 4:28-33.

72. Figure 2 shows the corresponding structure for dummy column 17. Voltage source $V_{REF}$ and transistor 36 are coupled in series to provide a reference voltage to one or more dummy cells through conductor 37. *Id.* at 4:7-14 ("The conductor 37 is coupled to receive a reference voltage labeled '$V_{REF}$' via an N-channel transistor 36."), 4:28-33 ("[P]rior to a write operation, control signal WDSEL* is provided as a logic high voltage to cause transistor 36 to be conductive. Reference voltage $V_{REF}$ is provided to the supply terminals of each of the memory cells 30, 32, and 34 precharging the cells of dummy column 17 to $V_{REF}$ (ground)."); *see also, e.g., id.* at 4:3-7, 4:39-55, 6:22-31.

73. Figure 3 shows the corresponding structure for dummy row 70. Voltage source $V_{REF}$ and transistor 90 are coupled in series to provide a reference voltage to one or more dummy cells through conductor 71. *See, e.g., id.* at 5:61-64, 6:11-16 (comparable structure for dummy row 70 in Fig. 3).

74. VLSI broadly asserts that the corresponding structure is "a conductor, or equivalents thereof."

75. A conductor is simply a circuit component through which charge can be transmitted.

76. Although the specification discloses that certain specific conductors (conductors 37 and 71) play a role in precharging, they cannot perform precharging by themselves. Instead, they merely serve as a conduit linking the dummy cells to the voltage source providing the reference voltage.

77. Moreover, VLSI's proposal does not limit the structure to conductor 37 or conductor 71. The '485 patent discusses a wide variety of different types of conductors including many conductors that play no role in precharging the capacitance structure. These include, for

example, conductor 35, conductor 39, conductor 67, and conductor 69. *Id.* at 3:39-40, 5:20-23, Figs. 2, 3.

**F. Disputed Term: "first coupling means for coupling the power supply terminal to the first power supply line during the write operation for the second line of memory cells"**

78. I understand that the parties agree that this term should be construed as a means-plus-function term and agree that the function is "coupling the power supply terminal to the first power supply line during the write operation for the second line of memory cells." I understand that the parties disagree, however, as to what structure in the specification of the '485 patent is linked to that function.

79. I understand that Intel has proposed that the corresponding structure is:

> (1) transistor 52 and clamping circuit 46, configured to couple power supply voltage $V_{DD}$ and conductor 35, as shown in Figure 2 (if the second line of memory cells is SRAM column 15), and equivalents thereof; or alternatively (2) transistor 96 and a clamping circuit, configured to couple power supply voltage $V_{DD}$ and conductor 67, as shown in Figure 3 (if the second line of memory cells is SRAM row 68), and equivalents thereof

80. The specification clearly links each of the components identified in Intel's construction to the stated function. A person of ordinary skill in the art would understand, from reading the '485 patent that it discloses specific structures that couple the power supply terminal to the first power supply line. *Id.* at 3:45-55, 4:33-39, 5:30-35, 5:35-40, 6:16-22, Figs. 2, 3.

81. Figure 2 shows the corresponding structure for a columns of memory cells. As depicted in Figure 2 and described in the specification, transistor 52 and clamping circuit 46 are coupled in parallel between the power supply voltage and the first power supply line. *Id.* at 3:45-55. Both serve to couple the power supply voltage to the first power supply line, supplying the first line of memory cells and limiting any voltage drop on the conductor to a predetermined level.

82. Figure 3 shows the corresponding structure for a row of memory cells. AS shown in Figure 3 and described in the specification, both transistor 96 and a clamping circuit are coupled in parallel between the power supply voltage and the first power supply line. *Id.* at 6:16-22. These are the structures identified by Intel.

83. VLSI broadly asserts that the corresponding structure is a "switching circuit." The specification does not describe a structure for such a circuit.

**G. Disputed Term: "second coupling means for coupling the second supply line to the first capacitance structure during the write operation for the second line of memory cells" (claim 17)**

84. I understand that the parties agree that this term should be construed as a means-plus-function term and agree that the function is "coupling the second supply line to the first capacitance structure during the write operation for the second line of memory cells." I understand that the parties disagree, however, as to what structure in the specification of the '485 patent is linked to that function.

85. I understand that Intel has proposed that the corresponding structure is:

> (1) Transistor 54, configured to couple conductor 39 to conductor 37, as shown in Figure 2 (if the second line of memory cells is SRAM column 15), and equivalents thereof; or alternatively (2) transistor 94, configured to couple conductor 69 to conductor 71, as shown in Figure 3 (if the second line of memory cells is SRAM row 68), and equivalents thereof

86. The specification clearly links each of the components identified by Intel to the stated function. A person of ordinary skill in the art would understand, from reading the '485 patent, that it discloses specific structures that couple the power supply terminal to the first power supply line. *Id.* at 4:14-23, 4:33-39, 5:65-6:6, 6:16-22.

87. Figure 2 shows the corresponding structure when the second supply line is coupled to a dummy column. The specification explains that "transistor 54 is used to couple conductor 37

to conductor 29" and this transistor becomes conductive "during the write operation." *Id.* at 4:15-39.

88. Figure 2 shows the corresponding structure when the second supply line is coupled to a dummy row rather than a dummy column. The specification explains that transistor 94, when a dummy row is used instead of a dummy column. *Id.* at 5:66-6:3, 6:36-46.

89. VLSI broadly asserts that the corresponding structure is a "switching circuit." The specification does not describe a structure for such a circuit.

**H. Disputed Term: "decoupling means for decoupling the first power supply line from the second line of memory cells during the write operation for the second line of memory cells" (claim 17)**

90. I understand that the parties agree that this term should be construed as a means-plus-function term and agree that the function is "decoupling the first power supply line from the second line of memory cells during the write operation for the second line of memory cells."

91. I understand that Intel contends that the '485 specification does not disclose any corresponding structure for this term. I further understand that VLSI asserts that the corresponding structure is "a switching circuit, or equivalents thereof."

92. At the time of the '485 patent's filing and continuing through today, a person of ordinary skill in the art would understand that the specification of the '485 patent discloses no structure for decoupling the first power supply line from the second line of memory cells. The specification does not disclose any examples where the ***first*** power supply line and ***second*** line of memory are coupled together. Instead, the ***first*** line of memory cells is coupled to the ***first*** power supply line, and the ***second*** line of memory is coupled to the ***second*** power supply line. '485 patent at Abstract. There accordingly is no need to decouple the first power supply line from the second line of memory cells because they are never coupled in the first place, and the specification does not disclose a structure for accomplishing this. A person of ordinary skill in the art would

not be able to identify any structure in the '485 patent that performs the function of "decoupling the first power supply line from the second line of memory cells."

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